IN THE SPECIFICATION

Please amend the paragraph at page 2, lines 12-19, as follows:

The control circuit 1 controls a gate voltage VGP of the PMOS transistor P1 and a gate voltage VGN of the NMOS transistor N1, and has the NAND gate G1 for inverting and outputting a control signal EN and an inverter INV1 for inverting and outputting an output of the NAND gate G1. The PMOS transistor P1 is turned on/off by the output of the NAND gate G1, and the NMOS transistor N1 is turned on/off by the output of the inverter INV1. The diode D1 is connected to the power supply line of the NAND gate G1 and the inverter INV1.

Please amend the paragraph at page 3, lines 21-34, as follows:

For example, when the signal voltage supplied to the first terminal I/O rises sharply, a time lag occurs until when the PMOS transistor P1 turns off. Accordingly, the signal is transmitted [[o]] to the second terminal, and the second terminal discharges electric charge with time constant of the resistance load and capacitance load. However, when frequency of the signal transmitted and received between the first and second terminals I/O and O/I is high, before discharge is completely finished, operations in which next signal is supplied to the first terminal and again the second terminal is discharged are repeated. Because of this, the second terminal is maintained in a state of high level, and the signal transmission path between the first and second terminals is not cut off.

Please amend the paragraph at page 4, lines 14-18, as follows:

Because of this, the size of the N well NW shown in Fig. 9 becomes large, and the capacitance (about 5 pF) of the capacitor C for the semiconductor substrate also becomes

large. Accordingly, delay of about 5 ns occurs due to resistance component (about 1kΩ) of the N well NW and a time constant.

Please amend the paragraph at page 8, lines 7-14, as follows:

Fig. 3 is a diagram showing an example of schematic structure of a semiconductor substrate on which the analog switch circuit of Fig. 1 is formed. As shown in Fig. 3, a P well PW and an N wells NW1 and NW2 are formed on the P type substrate [[10]] 3. The NMOS transistor N1 is formed on the P well PW, the PMOS transistor P1 and the diodes D2, D5 and D6 are formed on the N well NW1, and the control circuit 1 and the diodes D1, D3 and D4 are formed on the N well NW2.

Please amend the paragraph at page 8, lines 15-23, as follows:

Next, operation of the analog switch circuit of Figs. 1-3. First of all, operation in the case that the power supply voltage is supplied will be described. If the control signal EN is in high level, the output of the NAND gate G1 is in low ~~lever.~~ level, and the output of the inverter INV1 is in high level. Because of this, the PMOS transistor P1 and the NMOS transistor N1 turn on, and signal transmission is bi-directional performed between the first terminals I/O and O/I.

Please amend the paragraph at page 8, lines 24-29, as follows:

Furthermore, if the control signal [[En]] EN is in low level, the output of the NAND gate G1 becomes high level, and the output of the inverter INV1 becomes low level. Because of this, the PMOS transistor P1 and the NMOS transistor N1 turn off, and the signal transmission between the first and second terminals I/O and O/I is cut off.

Please amend the paragraph at page 8, line 36 to page 9, line 7, as follows:

At this time, when a voltage higher than the power supply voltage is supplied to the first [[and]] terminal I/O or the second ~~terminals I/O and~~ terminal O/I, the cathode voltage of the diode D1 rises via a diode D3. Because of this, the output of the ~~NMOS transistor N1~~ NAND gate G1 becomes high level, and the PMOS transistor P1 turns off. When the PMOS transistor P1 turns off, the signal transmission between the first and second terminals I/O and O/I is surely cut off.

Please amend the paragraph at page 9, lines 14-25, as follows:

That is, according to the present embodiment, two N wells NW1 and NW2 are provided. That is, the N well NW2 in which the diodes D1, D3 and D4 are formed are provided separate from the N well NW1 in which the PMOS transistor P1 is formed. Sizes of the N wells NW1 and NW2 are smaller than that of the conventional N well shown in Fig. 8. Accordingly, the capacitance of the capacitor C1 and the capacitance of the capacitor C2 are much smaller than the capacitance of the capacitor C of Fig. 8. More specifically, the capacitor C2 between the N well NW2 and the p type semiconductor substrate is 1/10 times of that of Fig. 8, i.e. about 0.5 pF. Accordingly, a time when sharp voltage rising of the first and second terminals I/O and O/I is transmitted to the power supply terminal of the NAND gate G1 is largely shortened, i.e. about 0.5 ns.

Please amend the paragraph at page 10, lines 11-13, as follows:

A switch circuit according to a second embodiment of the present invention constitutes the diodes ~~D1-D6~~ D1-D4 of Fig. 1 by MOS transistors.

Please amend the paragraph at page 10, lines 14-18, as follows:

Fig. 4 is [[a]] an analog switch circuit according to the second embodiment of the present invention. In the analog switch circuit of Fig. 4, the diodes ~~D1-D6~~ D1-D4 are composed of MOS transistors ~~M1-M6~~ M1-M4. In these MOS transistors, source terminals are shortcut to the corresponding gate terminals.